Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-32 (Canceled)

33. (Original) A monolithic three dimensional array of field effect transistors, comprising:

(a) a substrate;

(b) a plurality of first rails disposed at a first height relative to the substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

(c) a plurality of second rails disposed at a second height different from the first height, and in a second direction different from the first direction,

wherein each of the plurality of second rails comprises:

a second lightly doped semiconductor channel layer of a second conductivity type located in contact with the first rails;

a second heavily doped semiconductor layer of the first conductivity type; and

a second gate insulating layer between and in contact with the second channel layer and the second heavily doped layer of the first conductivity type;

a second heavily doped semiconductor layer of the second conductivity type electrically connected to the second heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer;

(d) a plurality of third rails disposed in the first direction at a third height relative to the substrate, wherein each of the plurality of third rails comprises:

a third lightly doped semiconductor channel layer of the first conductivity type located in contact with the second heavily doped layer of the second conductivity type in the second rails;

a third heavily doped semiconductor layer of the second conductivity type;

a third heavily doped semiconductor layer of the first conductivity type electrically connected to the third heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer; and

a third gate insulating layer between and in contact with the channel layer and the third heavily doped layer of the second conductivity type.

34. (Original) The array of claim 33, further comprising a plurality of fourth rails disposed in the second direction at a fourth height relative to the substrate, wherein each of the plurality of fourth rails comprises:

a fourth lightly doped semiconductor channel layer of the second conductivity type in contact with the third heavily doped layer of the first conductivity type in the third rails;

a fourth heavily doped semiconductor layer of the first conductivity type; and

a fourth gate insulating layer between and in contact with the fourth channel layer and the fourth heavily doped layer of the first conductivity type; and

a fourth heavily doped semiconductor layer of the second conductivity type electrically connected to the fourth heavily doped semiconductor layer of the first conductivity type by a metal or a metal silicide layer.

35. (Original) The array of claim 34, wherein:

the first heavily doped semiconductor layer of the first conductivity type comprises source or a drain regions of a plurality of first transistors;

the second heavily doped semiconductor layer of the first conductivity type comprises gate electrodes of the first transistors;

the second heavily doped semiconductor layer of the second conductivity type comprises source or drain regions of a plurality of second transistors;

the third heavily doped semiconductor layer of the second conductivity type comprises gate electrodes of the second transistors; and

the third heavily doped semiconductor layer of the first conductivity type comprises source or drain regions of a plurality of third transistors.

36. (Original) The array of claim 35, wherein:

one or more of the semiconductor layers in the first through fourth rails is a polysilicon layer; and

the pluralities of first, second and third transistors comprise top gate staggered thin film transistors located above an insulating substrate or above an insulating layer formed over a silicon substrate.

37. (Original) The array of claim 36, further comprising:

planarized insulating fill located between adjacent first rails, between adjacent second rails, between adjacent third rails, and between adjacent fourth rails;

a first insulating isolation layer located between the first rails and the second rails;

a second insulating isolation layer located between the second rails and the third rails;

a third insulating isolation layer located between the third rails and the fourth rails;

a plurality of first openings in the first isolation layers through which the second lightly doped semiconductor layers of the second conductivity type in the second rails contact the first heavily doped semiconductor layers of the first conductivity type in the first rails;

a plurality of second openings in the second isolation region through which the third lightly doped semiconductor layers of the first conductivity type in the third rails contact the second heavily doped semiconductor layers of the second conductivity type in the second rails; and

a plurality of third openings in the third isolation layer through which the fourth lightly doped semiconductor layers of the second conductivity type in the fourth rails contact the first heavily doped semiconductor layers of the first conductivity type in the first rails.

38. (Original) A semiconductor device, comprising:

a first field effect transistor of a first polarity; and

a second field effect transistor of a second polarity;

wherein a gate electrode of the first transistor is electrically connected to a source or drain of the second transistor without any lateral interconnects.

Claims 39-49 (Canceled)

50. (Original) A method of making a monolithic three dimensional field effect transistor array, comprising:

forming a plurality of first rails disposed at a first height relative to a substrate in a first direction, wherein each of the plurality of first rails comprises a first heavily doped semiconductor layer of a first conductivity type;

forming a first insulating isolation layer over the first plurality of rails;

patterning the first isolation layer to form a plurality of first openings exposing upper portions of adjacent first rails;

forming a second lightly doped semiconductor layer of a second conductivity type over the patterned isolation layer such that transistor channel portions in the second lightly doped layer of the second conductivity type contact the first heavily doped layer of the first conductivity type through the first openings;

forming a second gate insulating layer over the second lightly doped semiconductor layer of the second conductivity type;

forming a second heavily doped semiconductor layer of the first conductivity type over the second gate insulating layer; and

patterning the second heavily doped layer of the first conductivity type, the second gate insulating layer, and the second lightly doped layer of the second conductivity type to form a plurality of second rails extending in a second direction different from the first direction.

51. (Original) The method of claim 50, further comprising:

forming a second insulating isolation layer over the plurality of second rails;

patterning the second isolation layer to form a plurality of second openings exposing upper portions of adjacent second rails;

forming a third lightly doped semiconductor layer over the patterned second isolation layer such that transistor channel portions of the second lightly doped layer contact the second rails through the second openings;

forming a third gate insulating layer over the third lightly doped semiconductor layer;

forming a third heavily doped semiconductor layer over the third gate insulating layer; and

patterning the third heavily doped layer, the third gate insulating layer and the third lightly doped layer to form a plurality of third rails extending in the first direction.

52. (Original) The method of claim 51, further comprising forming a plurality of fourth rails extending in the second direction in contact with the third rails.

53. (Original) The method of claim 51, further comprising:

forming a first insulating fill layer between adjacent first rails;

polishing the first insulating fill layer to expose the first rails using the first rails as a polish stop;

forming a second insulating fill layer between adjacent second rails;

polishing the first insulating fill layer to expose the second rails using the second rails as a polish stop;

forming a third insulating fill layer between adjacent third rails; and

polishing the third insulating fill layer to expose the third rails using the third rails as a polish stop.

54. (Original) The method of claim 53, wherein the step of forming the first rails further comprises:

forming a second heavily doped polysilicon layer over the substrate;

forming a first metal or metal silicide layer over the second polysilicon layer;

forming the first heavily doped semiconductor layer on the first metal or metal silicide layer; and

patterning the first semiconductor layer and the second polysilicon layer and the first metal or metal silicide layers.

55. (Original) The method of claim 51, wherein:

the third lightly doped semiconductor layer comprises a third lightly doped amorphous silicon or polysilicon layer of the first conductivity type; and

the third heavily doped semiconductor layer comprises a third heavily doped polysilicon layer of the second conductivity type formed on the third gate insulating layer.

56. (Original) The method of claim 55, further comprising:

forming a second metal or metal silicide layer on the second heavily doped semiconductor layer of the first conductivity type;

forming a second heavily doped semiconductor layer of the second conductivity type on the second metal or metal silicide layer;

patterning the second metal or metal silicide layer and the second heavily doped semiconductor layer of the second conductivity type during the step of patterning to form the second rails;

forming a third metal or metal silicide layer on the third heavily doped polysilicon layer of the second conductivity type;

forming a third heavily doped semiconductor layer of the first conductivity type on the third metal or metal silicide layer; and

patterning the third metal or metal silicide layer and the third heavily doped semiconductor layer of the first conductivity type during the step of patterning to form the third rails.

57. (Original) The method of claim 56, wherein all layers in the second rails are patterned by etching during one etching step.

58. (Original) The method of claim 56, further comprising:

forming vias which extend through the second gate insulating layer and the second lightly doped layer to the first rails;

depositing the second heavily doped layer of the first conductivity type into the vias such that the second heavily doped layer of the first conductivity type contacts the first heavily doped layer of the first conductivity type;

forming vias which extend through the third gate insulating layer and the third lightly doped layer to the second rails; and

depositing the third heavily doped layer of the second conductivity type into the vias such that the third heavily doped layer of the second conductivity type contacts the second heavily doped layer of the second conductivity type.

59. (Original) The method of claim 51, wherein:

the third lightly doped semiconductor layer comprises a third lightly doped amorphous silicon or polysilicon layer of the second conductivity type;

the third heavily doped semiconductor layer comprises a third heavily doped polysilicon layer of the first conductivity type formed on the third gate insulating layer.

60. (Original) The method of claim 59, further comprising:

forming a second metal or metal silicide layer on the second heavily doped semiconductor layer of the first conductivity type;

forming a fourth heavily doped semiconductor layer of the first conductivity type on the second metal or metal silicide layer;

patterning the second metal or metal silicide layer and the fourth heavily doped semiconductor layer of the first conductivity type during the step of patterning the second rails;

forming a third metal or metal silicide layer on the third heavily doped polysilicon layer of the first conductivity type;

forming a fifth heavily doped semiconductor layer of the first conductivity type on the third metal or metal silicide layer; and

patterning the third metal or metal silicide layer and the fifth heavily doped semiconductor layer of the first conductivity type during the step of patterning the third rails.

61. (Original) The method of claim 50, wherein all layers in the second rails are patterned by etching during one etching step.

62. (Original) A monolithic three-dimensional array of active devices comprising odd and even levels of field effect transistors, wherein:

odd levels comprise transistors of a first polarity;

even levels comprise transistors of a second polarity;

each transistor comprises a gate electrode, source, and drain, wherein the gate electrodes, sources, and drains of the transistors of at least two levels comprise polysilicon;

current flows between the source and the drain in a first direction through transistors of the first polarity; and

current flows between the source and the drain in a second direction not parallel to the first direction through transistors of the second polarity.

63. (Original) The array of claim 62, further comprising:

a substrate;

a plurality of first rails disposed at a first height above the substrate, extending in the first direction, said plurality of first rails comprising sources and drains of the first level of the transistors;

a plurality of second rails in contact with the first rails, at a second height different from the first height, extending in a second direction, said second rails comprising gate electrodes of the first level of transistors and further comprising sources and drains of the second level of transistors; and

a plurality of third rails in contact with the second rails, at a third height different from the second height, extending in the first direction, such that the second rails are located between the first rails and the third rails, said third rails comprising gate electrodes of the second level of transistors.

64. (Original) The array of claim 63, wherein the second direction is substantially orthogonal to the first direction.

Claims 65-72 (Canceled)